VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
B.E. (EEE) III Year II Semester Old Examinations, May/June-2019
Digital Signal Processing

Time: 3 hours

Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

1. State sampling theorem.

2. What are deterministic and random signals?

3. Compare Radix-2 DIT and DIF algorithms in computation of FFT.

4. Find the inverse DFT of $X[k] = \{3,4,5,6\}$

5. State convolution and multiplication properties of Z-transform.

6. Define region of convergence (ROC) in Z – domain.

7. Write the equation to find the order of Butterworth filter.

8. Compare Butterworth and Chebyshev IIR filters.

9. Explain about pin multiplexing.

10. Explain General Purpose Input Output (GPIO) functionality in DSP processors.

Part-B (5 × 10=50 Marks)

11.a) Examine the properties linearity and time or shift invariance for the system $y[n] = \cos(x[n])$ [5]

b) Draw discrete unit ramp sequence $r[n]$ and shifted sequence $r[n-K]$. [5]

12.a) Compare linear and circular convolution methods. [4]

b) Draw butterfly diagram for 8 point DFT using DIT algorithm. [6]

13.a) Compute Z-transform of $x[n] = \cos(\omega_0 n)u[n]$. [5]

b) Using one sided Z – transform, obtain unit step response of the system for $n \geq 0$ with difference equation $y[n] = 0.5y[n-1]+x[n]$, where $x[n]=(1/3)^n u[n]$ and $y[-1]=1$ [5]

14.a) Design a low-pass FIR digital filter whose frequency response is given by [6]
$H(e^{j\omega}) = 1, -\omega_c \leq \omega \leq \omega_c$
$0, \omega_c \leq |\omega| \leq \omega_s/2$

b) Apply bilinear transformation to $H_a(S) = 4/ (S+3)(S+4)$ to obtain transfer function of digital IIR filter. [4]

15.a) Define features of digital signal processors. [4]

b) Draw the architecture of TMS320LF2407 processor. [6]

16.a) Determine if the system $y(n) = x(n^2)$ is time invariant. [5]

b) Find convolution of $x_1[n] = \{1,-1,-2,3,-1\}$ and $x_2[n] = \{1,2,3\}$ using matrix method. [5]

17. Answer any *two* of the following:

a) Explain how stability is evaluated in Z – domain. [5]

b) Explain how FIR filter is designed using Kaiser window. [5]

c) Write short notes on watchdog timer and Phased Lock Loop in TMS320LF2407 processor. [5]